Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-12 (Canceled).

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13. (Original) A modular interconnection architecture for an expandable multiprocessor machine, based on a virtual bus hierarchy, comprising a given number of multiprocessor modules (QPi) , each module including a plurality of processors and associated cache memories organized into nodes (Nj) and distributed on at least two interconnection levels: a first interconnection level (MI) corresponding to interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) connecting the multiprocessor modules (QPi) to one another and handling the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to one another and handling the transactions between the nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, the same external interface (XI), and adapted to implement the same coherency control protocol for the cache memories of the processors.

14. (Original) A modular interconnection architecture according to claim 13, characterized in that each external connection node (NCEj) comprises two identical connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j) receiving and filtering transactions sent by the node (Nj) to which it is

connected, and the other agent (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which it is connected.

15. (Original) A modular interconnection architecture according to claim 13, characterized in that each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

16. (Original) A modular interconnection architecture according to claim 14, characterized in that each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

17. (Original) A modular interconnection architecture according to claim 14, characterized in that the first and second head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for blocks modified in their respective associative memories (DD'j and DD"j); modified data blocks in the first connection agent (NCS'j) being exported to the requesting multiprocessor module or modules and, conversely, modified data blocks in the second connection agent (NCS"j) being imported from the module or modules holding the blocks.

18. (Original) A modular interconnection architecture according to claim 13, characterized in that the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).

19. (Original) A modular interconnection architecture according to claim 14, characterized in that the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).

20. (Original) A modular interconnection architecture according to claim 15, characterized in that the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).

21. (Original) A modular interconnection architecture according to claim 16, characterized in that the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).

22. (Original) A modular interconnection architecture according to claim 17, characterized in that the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).

23. (Currently amended) A process for expanding the capacity of a machine comprising a first given number of processors on a first level (MI) organized into a first given number of multiprocessor modules (QPi) and capable of being inserted into an interconnection architecture comprising a modular interconnection architecture for an expandable multiprocessor machine, based on a virtual bus

hierarchy, comprising a given number of multiprocessor modules (QPi) ,each comprising a plurality of processors and associated cache memories organized into nodes (Nj) and distributed on at least two interconnection levels: a first interconnection level (MI) corresponding to interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) connecting the multiprocessor modules (QPi) to one another and handling the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to one another and handling the transactions between the nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, the same external interface (XI), and adapted to implement the same coherency control protocol for the cache memories of the processors, [[.]]characterized in that it consists of disconnecting one of the first-level multiprocessor modules (QPi) from its connection agent (NCSi) to free said connecting agent and of connecting, via said freed connection agent, a second given number of processors organized into a second given number of multiprocessor modules, also capable of being inserted into said interconnection architecture.

24. (Original) A process for expanding the capacity of a machine comprising a first given number of processors on a first level (MI) organized into a first given number of multiprocessor modules (QPi) and capable of being inserted into an interconnection architecture comprising a modular interconnection architecture for an expandable multiprocessor machine, based on a virtual bus hierarchy, comprising a

given number of multiprocessor modules (QPi) ,each comprising a plurality of processors and associated cache memories organized into nodes (Nj) and distributed on at least two interconnection levels: a first interconnection level (MI) corresponding to interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) connecting the multiprocessor modules (QPi) to one another and handling the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to one another and handling the transactions between the nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, the same external interface (XI), and adapted to implement the same coherency control protocol for the cache memories of the processors, each external connection node (NCEj) comprises two identical connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j) receiving and filtering transactions sent by the node (Nj) to which it is connected, and the other (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which it is connected, characterized in that it consists of disconnecting one of the first-level multiprocessor modules (QPi) from its connection agent (NCSi) to free said connecting agent and of connecting, via said freed connection agent, a second given number of processors organized into a second given number of multiprocessor modules, also capable of being inserted into said interconnection architecture.

25. (Original) A process for expanding the capacity of a machine comprising a first given number of processors on a first level (MI) organized into a

first given number of multiprocessor modules (QPi) and capable of being inserted into an interconnection architecture comprising a modular interconnection architecture for an expandable multiprocessor machine, based on a virtual bus hierarchy, comprising a given number of multiprocessor modules (QPi) ,each comprising a plurality of processors and associated cache memories organized into nodes (Nj) and distributed on at least two interconnection levels: a first interconnection level (MI) corresponding to interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) connecting the multiprocessor modules (QPi) to one another and handling the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to one another and handling the transactions between the nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, the same external interface (XI), and adapted to implement the same coherency control protocol for the cache memories of the processors, characterized in that it consists of disconnecting one of the first-level multiprocessor modules (QPi) from its connection agent (NCSi) to free said connecting agent and of connecting, via said freed connection agent, a second given number of processors organized into a second given number of multiprocessor modules, also capable of being inserted into said interconnection architecture, each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories

(DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

26. (Original) A process according to claim 24, characterized in the connection agents (NCS'j) and (NCS"j) respectively comprise an associative memory (DD'j) and (DD"j) with a fixed size determined as a function of the number of processors in the multiprocessor module (HBj) to which the connection agents (NCS'j) and (NCS"j) are connected, the state of the associated memories (DD'j) and (DD"j) being indicative of the presence of the last modified data blocks executed or conversely imported.

27. (Currently amended) A process for expanding the capacity of a machine according to claim 24 wherein the first and second head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for blocks modified in their respective associative memories (DD'j and DD"j); modified data blocks in the first connection agent (NCS'j) being exported to the requesting multiprocessor module or modules and, conversely, modified data blocks in the second connection agent (NCS"j) being imported from the module or modules holding the blocks., ~~characterized in that it consists of disconnecting one of the first-level multiprocessor modules (QPi) from its connection agent (NCSi) to free said connecting agent and of connecting, via this freed connection agent, a second given number of processors organized into a second given number of multiprocessor modules, also capable of being inserted into said interconnection architecture comprising a modular interconnection architecture.~~

28. (Currently amended) A process for expanding the capacity of a machine according to claim 24 wherein the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI)~~, characterized in that it consists of disconnecting one of the first-level multiprocessor modules (QPi) from its connection agent (NCSi) to free said connecting agent and of connecting, via this freed connection agent, a second given number of processors organized into a second given number of multiprocessor modules, also capable of being inserted into said interconnection architecture.~~

29. (Original) A process according to claim 23, characterized in that, the second given number of processors being organized into a second given number of multiprocessor modules on a second level (SI), it consists of connecting it to the connection agent (NCSi) of the first given number of processors on the first level (MI) through one of the connection agents (NCS"j) on the second level.

30. (Original) A process according to claim 29, characterized in that, the second given number of processors also being on the first level (MI), and further comprising connecting the respective connection agents (NCS') to the first and second given numbers of processors, the second level (SI) being reduced to a single link.

31. (Currently amended) An expandable ~~multi node~~multinode multiprocessor machine, comprising an interconnection architecture including a given number of multiprocessor modules including a modular interconnection architecture for an expandable multiprocessor machine, based on a virtual bus hierarchy, comprising a given number of multiprocessor modules (QPi) , each module including

a plurality of processors and associated cache memories organized into nodes (Nj) and distributed on at least two interconnection levels: a first interconnection level (MI) corresponding to interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) connecting the multiprocessor modules (QPi) to one another and handling the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to one another and handling the transactions between the nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, the same external interface (XI), and adapted to implement the same coherency control protocol for the cache memories of the processors.

32. (Original) An expandable multinode multiprocessor machine as set forth in claim 31, characterized in that each external connection node (NCEj) comprises two identical connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j) receiving and filtering transactions sent by the node (Nj) to which it is connected, and the other agent (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which it is connected.

33. (Original) An expandable multinode multiprocessor machine as set forth in claim 31, characterized in that each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi)

is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

34. (Original) An expandable multinode multiprocessor machine as set forth in claim 31, characterized in that each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

35. (Original) An expandable multinode multiprocessor machine as set forth in claim 31, characterized in that the first and second head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for blocks modified in their respective associative memories (DD'j and DD"j); modified data blocks in the first connection agent (NCS'j) being exported to the requesting multiprocessor module or modules and, conversely, modified data blocks in the second connection agent (NCS"j) being imported from the module or modules holding the blocks.

36. (Original) An expandable multinode multiprocessor machine as set forth in claim 31, characterized in that the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).

37 (Currently amended) A process for tracing data blocks in an interconnection architecture for an expandable microprocessor machine, based on a virtual bus hierarchy, comprising a given number of multiprocessor modules (QPi)

,each module including a plurality of processors and associated cache memories organized into nodes (Nj) and distributed on at least two interconnection levels: a first interconnection level (MI) corresponding to interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) connecting the multiprocessor modules (QPi) to one another and handling the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to one another and handling the transactions between the nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, the same external interface (XI), and adapted to ~~mplement~~implement the same coherency control protocol for the cache memories of the processors, comprising duplicating on the first level in the associative memories (DDi) only modified data blocks in the cache memories of the multiprocessor modules (QPi) and tracing only the modified blocks inside the node (Nj).

38. (Original) A process for tracing data blocks as set forth in claim 37 wherein each external connection node (NCEj) comprises two identical connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j) receiving and filtering transactions sent by the node (Nj) to which it is connected, and the other agent (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which it is connected.

39. (Original) A process for tracing data blocks as set forth in claim 37 wherein each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

40. (Original) A process for tracing data blocks as set forth in claim 38, characterized in that the first and second head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for blocks modified in their respective associative memories (DD'j and DD"j); modified data blocks in the first connection agent (NCS'j) being exported to the requesting multiprocessor module or modules and, conversely, modified data blocks in the second connection agent (NCS"j) being imported from the module or modules holding the blocks

41. (Original) A process for tracing data blocks as set forth in claim 38, characterized in that the first and second head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for blocks modified in their respective associative memories (DD'j and DD"j); modified data blocks in the first connection agent (NCS'j) being exported to the requesting multiprocessor module or modules and, conversely, modified data blocks in the second connection agent (NCS"j) being imported from the module or modules holding the blocks.

42. (Currently amended) A process for tracing data blocks as set forth in claim ~~13~~37, characterized in that the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).

43. (Original) A process for tracing data blocks in a modular interconnection architecture for an expandable multiprocessor machine, based on a virtual bus hierarchy, comprising a given number of multiprocessor modules (QPi) , each module including a plurality of processors and associated cache memories organized into nodes (Nj) and distributed on at least two interconnection levels: a first interconnection level (MI) corresponding to interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with one another, the first interconnection level (MI) comprising connection agents (NCSi) connecting the multiprocessor modules (QPi) to one another and handling the transactions between the multiprocessor modules (QPi), the second interconnection level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to one another and handling the transactions between the nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, the same external interface (XI), and adapted to implement the same coherency control protocol for the cache memories of the processors, characterized in that it consists, on the second level (SI), of duplicating in the associative memories (DD'j and DD"J) of the connection agents (NCS' and NCS"j) of each external connection node (NCEj) only the modified blocks exported, or conversely imported, and of tracing only the modified blocks exported, or conversely imported, between each node (Nj) of the machine.

44. (Original) A process for tracing data blocks as set forth in claim 43, wherein each external connection node (NCEj) comprises two identical connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j) receiving and filtering transactions sent by the node (Nj) to which it is connected, and the other agent (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which it is connected.

45. (Original) A process for tracing data blocks as set forth in claim 43, wherein each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

46. (Original) A process for tracing data blocks as set forth in claim 44, wherein each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi).

47. (Original) A process for tracing data blocks as set forth in claim 44, wherein the first and second head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for blocks modified in their respective associative memories (DD'j and DD"j); modified data blocks in the first connection agent (NCS'j) being exported

to the requesting multiprocessor module or modules and, conversely, modified data blocks in the second connection agent (NCS"j) being imported from the module or modules holding the blocks.

48. (Original) A process for tracing data blocks as set forth in claim 43, wherein the second interconnection level (SI) has a latency that is double the latency of the first interconnection level (MI).